White Paper

Thin-Film-Transistor (TFT) LCD Display Control Electronics Design and Operation

Revision 1.0

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1   TFT OVERVIEW

Thin-Film Transistor (TFT) displays are growing in popularity due to their resolution and speed. Today's LCD televisions and monitors are built using TFT technologies. The structure and operation of a TFT display is shown in Figure 1.
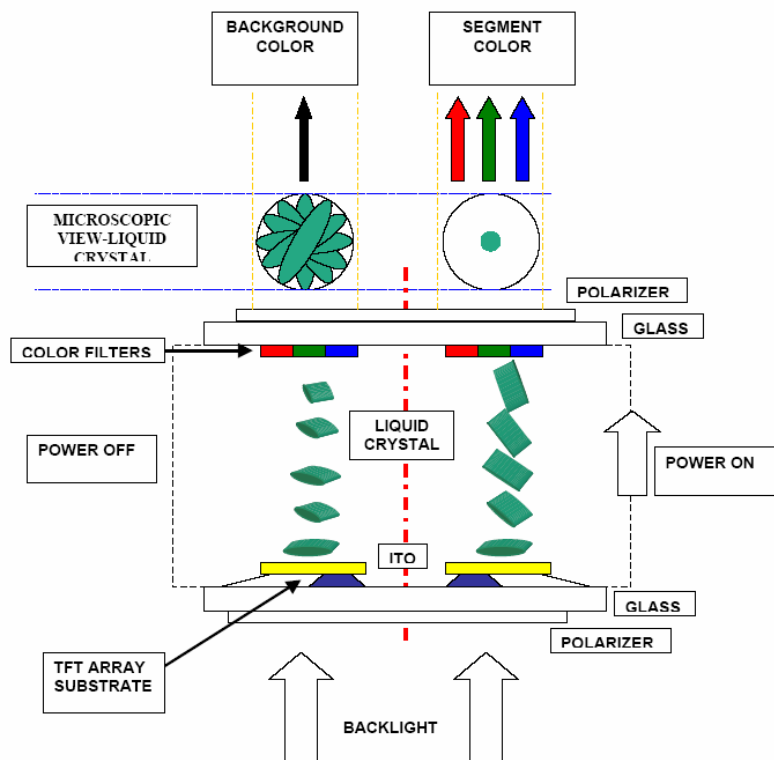

Figure 1: TFT LCD structure and operation

Figure 1 demonstrates the electrochemical operation characteristics of a TFT display. The drive electronics of a TFT activate the TFT array substrate, resulting in an induced electromagnetic field that affects the liquid crystal. The liquid crystal is twisted in response to the induced E-field, allowing light to shine through the glass sandwich. The light is modulated by the color filters to output the desired color. Since TFT arrays are semiconductor-fabricated transistors, they react on a microsecond scale, whereas traditional ITO-based designs in conventional graphic STN LCDs react on a millisecond scale. This thousand-fold increase is achieved by creating localized activations across the individual TFT pixel transistors rather than grid-based activations of an ITO-based graphic LCD.

In this paper, we will focus on the drive electronics required in a TFT. The main blocks of the drive system for a TFT are: Controller, Greyscale generator, and Voltage Drive generator.
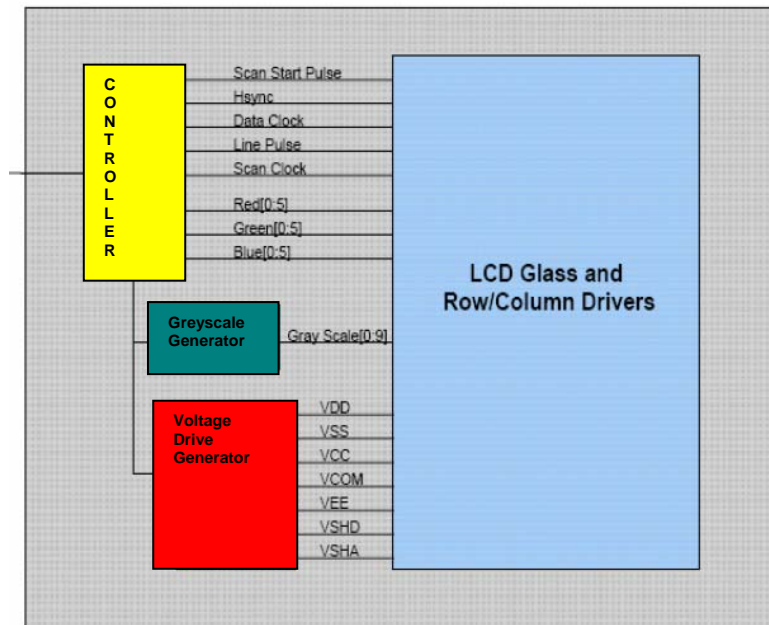
Figure 2: Block Diagram: Elements of TFT drive electronics

The Controller logic block controls the instruction and clock signals to the TFT glass's row and column drivers. The Controller logic block also includes a timing subsection that generates the correct signal cycles to drive the TFT correctly. The Controller logic block will be detailed in Section 2.

The Greyscale Generator logic block generates the target reference voltages across a voltage divider circuit to control the brightness and clarity of each color pixel. The Controller logic block then uses the voltage levels generated by the greyscale generator block and sends them to individual transistor pixels to control the brightness and clarity of the color output. The Greyscale Generator logic block will be detailed in Section 3.

The Voltage Drive Generator logic block generates the necessary TFT drive voltages for the row/column drivers to drive the TFT LCD. The Voltage Drive logic block creates the necessary voltage waveforms to achieve (1) color output stability to alleviate flickering and inconsistent color, and (2) liquid crystal stability to prevent display damage due to localized net voltage build-up. The Voltage Drive logic block will be detailed in Section 4. The Controller logic block controls the Voltage Drive block to maintain the correct timing waveforms of the drive voltages and to control the On/Off function through Power Sequencing, which will be detailed in Section 5.

2 TFT CONTROLLER LOGIC

2.1 DRIVERS-ONLY TFT LCD DISPLAYS

Figure 3: TFT Row/Column Driver Interface

In some applications, engineers prefer to use a drivers-only TFT LCD. Drivers-only interface requires the product engineers to essentially build a TFT controller circuit with control software code programmed into their microprocessor or microcontroller. Therefore, the timing, greyscale generation and voltage drive functions are controlled directly through the application.

Design constraints drive the need for drivers-only TFT LCDs. Many PDA and portable applications have tight mechanical constraints, so product designers cannot accommodate a full-sized TFT LCD module with embedded drive electronics. Instead, they move the drive electronics onto their application and utilize their microcontroller or microprocessor to code embedded software to mimic the TFT control drive electronic functions. This allows them to create a thin, tight package to fit their needs.

Another reason for using drivers-only TFT is cost. By placing the TFT drive electronics onto their application, the product designers can save money by creating a custom board with all electronics and using a drivers-only TFT LCD. By spending more hardware and embedded software development time upfront through a custom design, the product designer can lower the cost of the product at mass production, in addition to allowing their buyers the flexibility of using TFT LCD panels from multiple vendors.
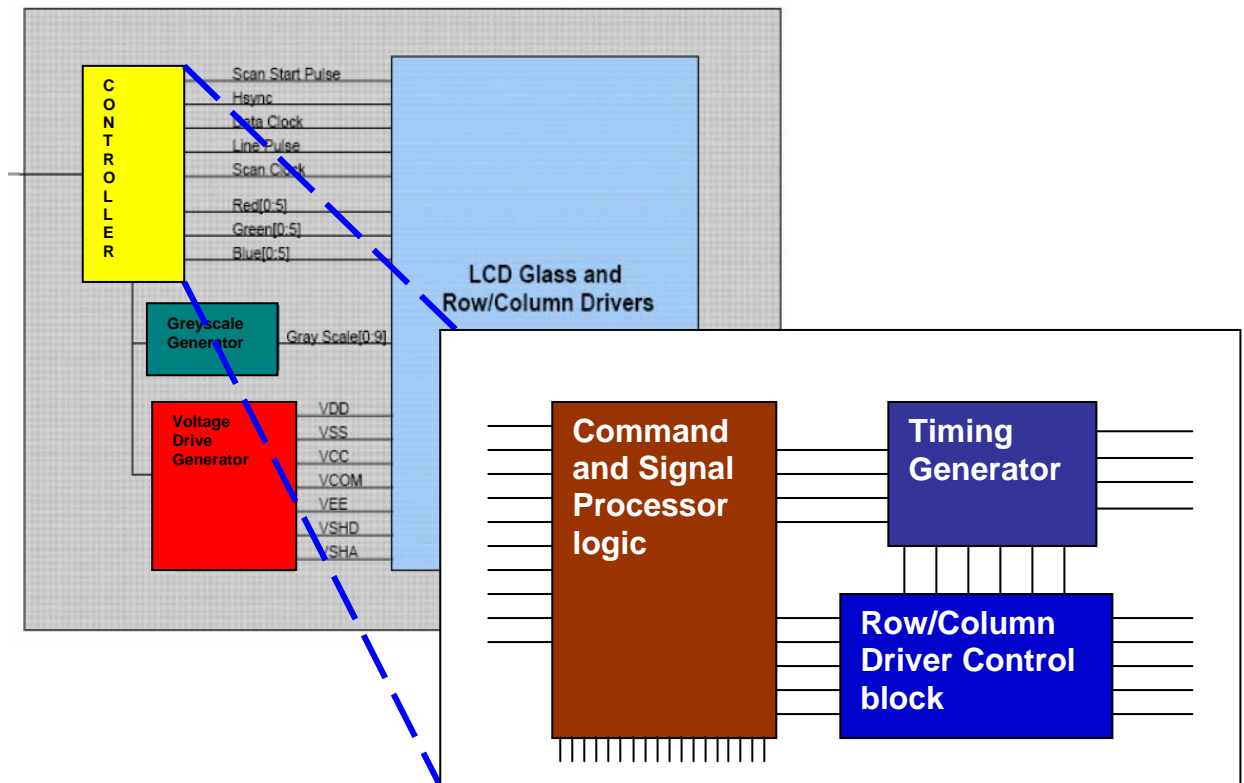
2.2 CONTROLLER BLOCK DIAGRAM

Figure 4: Controller logic subsections

The TFT controller logic block is comprised of 3 blocks; the command and signal processor logic, the timing generator logic and the row/column control logic.

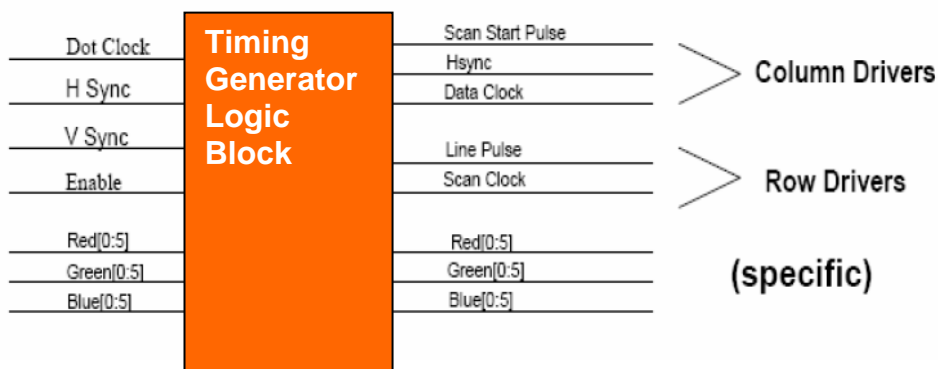The timing generator logic is shown in Figure 5.

Figure 5: Timing generator logic block

The timing generator logic takes the global timing signals from the application input and generates the specific signal waveforms required for the TFT's row and column drivers. In addition, the timing generator logic block interacts with the row/column driver control block to ensure the driver control signals are aligned to the specific signal waveforms for proper row/column driver operation.

The command and signal processor logic block coordinates the TFT's input signals and generates the required waveforms to the timing generator logic, the row/column driver logic, the greyscale generator logic and the voltage drive logic.

The command and signal processor logic block coordinates with the row/column driver logic block through the signals in Figure 6.

Figure 5: [Command and Signal Processor] logic and
Row/Column driver signals

Below are some of the interface signals used in a TFT display.

-UBR and LBR control the scan direction of the display.
-SPR and SPL are the start signals for the column drive shift register. Only one signal will be active during operation, depending on the scan direction.
-CLK is the dot clock for the column drivers.
-LP is similar to the Hsync signal: it is the latching signal for the column drivers.
-SPS is the start pulse for the gate (row) drivers. SPS is similar to the Vsync signal.
-CLS is the clock signal for the gate drivers. This signal increments the row driver counter.
-REV and REVV0 are the toggle signals for the greyscale generator logic block.

These signals are processed by the Command and Signal Processor logic block, and then the instructions are sent to the greyscale generator logic block.

These signals are used in most TFT panels; nomenclature is vendor-specific.
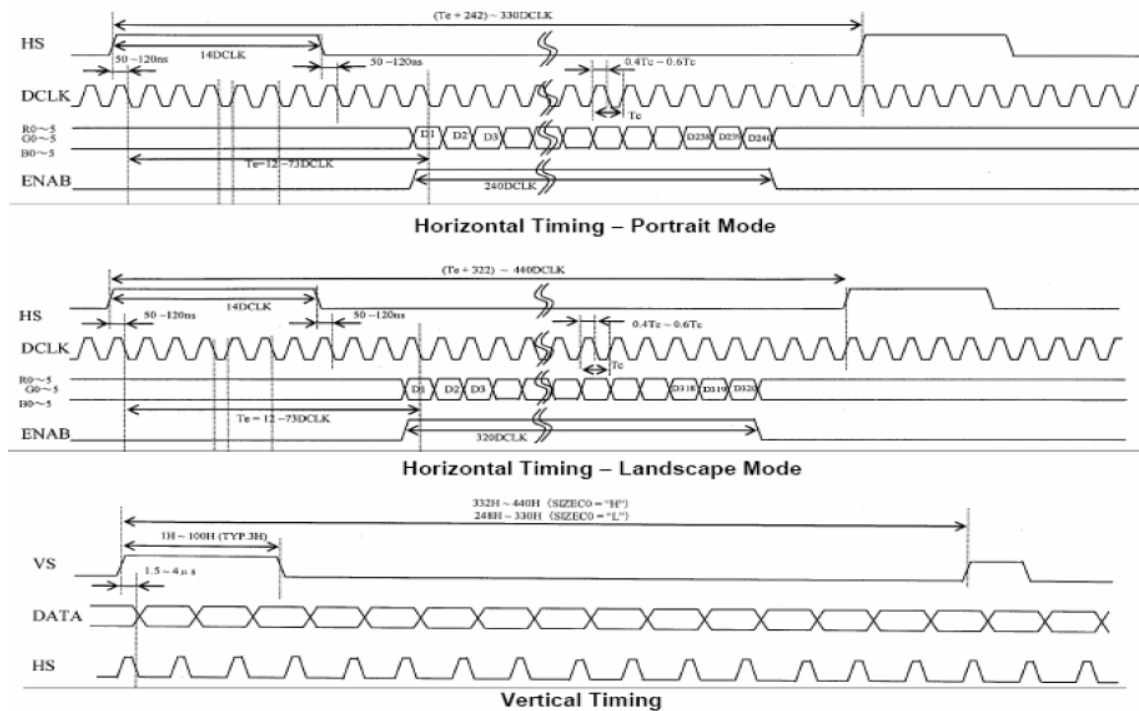
2.3 INPUT TIMING WAVEFORMS - EXAMPLE

Figure 6: Input Timing Waveforms

These waveforms are examples of the required input waveforms for a TFT with built-in controller. Most TFT displays offer the choice of portrait or landscape mode graphics; the waveforms depend on the graphic mode used as well.

Since landscape mode require more horizontal pixels than portrait mode, it requires longer instruction cycle times. Note the differences between the horizontal-portrait (top) and horizontal-landscape (middle) waveforms. Most of the instructions, including the RGB inputs, are the same, except for ENAB (ENABLE) cycle time. For landscape mode, ENAB requires a longer cycle at 320 DCLK whereas in portrait mode, ENAB requires only 240 DCLK. This translates to a longer instruction cycle time, since in landscape mode the total instruction cycle is 440 DCLK while in portrait mode, it is 330 DCLK.

The same applies to the vertical timing (bottom) waveform. In portrait mode, the instruction cycle time is 332~440H while in landscape mode, it is 248~330H.

The timing issues above are relative values; however, this example is a reminder that using driver-only TFT LCD displays require more intensive signal timing management than with controller-only TFT displays, which only require attention to overall instruction cycles.

3 GREYSCALE GENERATOR/PANEL STABILITY

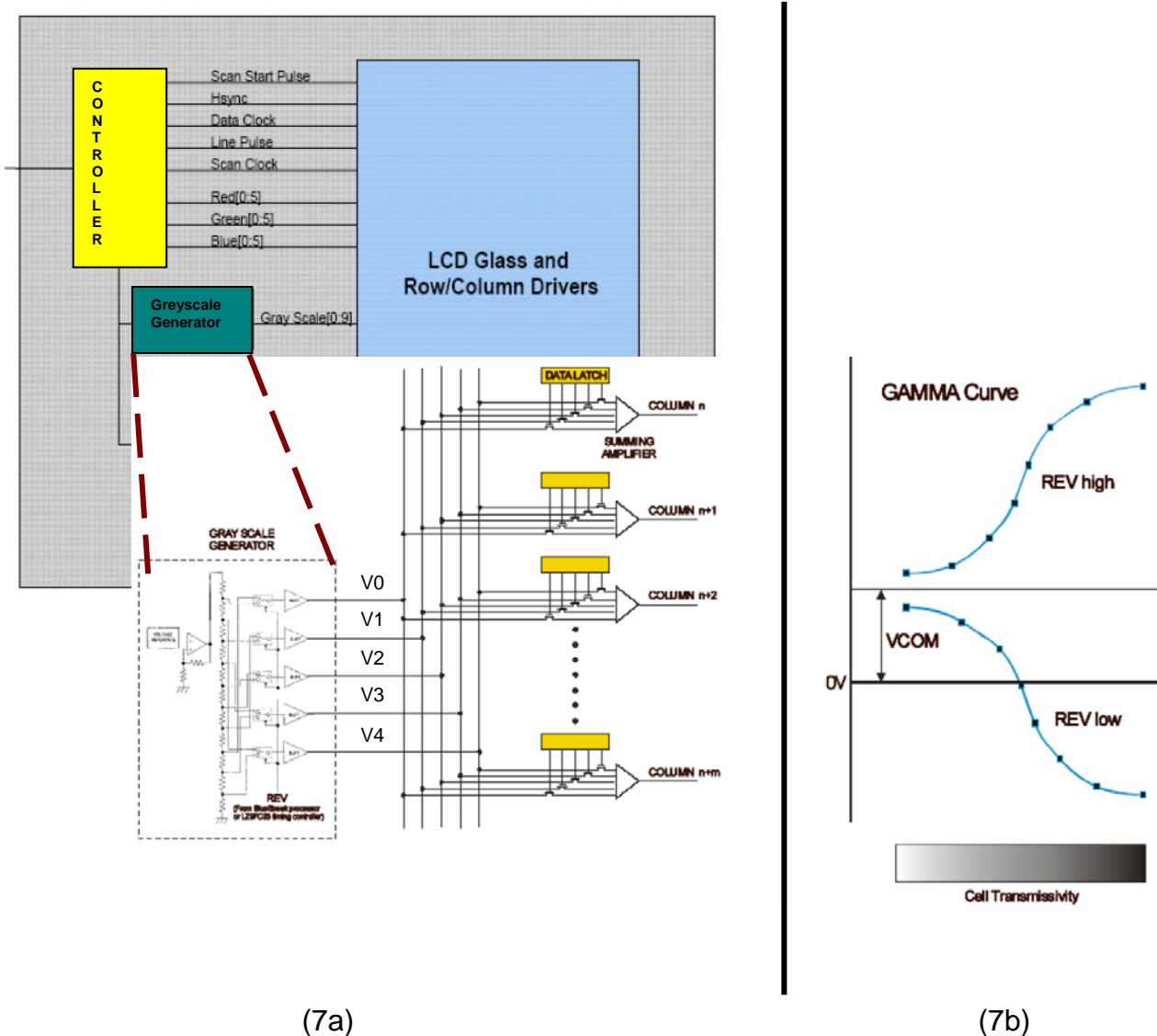## 3.1 Circuit and Operation

(7a)   (7b)

Figure 7: Greyscale Generator Circuit, with the voltage latch
and summing amplifier circuitry inside the column drivers

Figure 7a is an example of the greyscale generator circuit. The greyscale generator consists of an op-amp network that generates distinct V0-V4 voltages. These V0-V4 voltages are then paralleled into the summing amplifier circuits (D/A converter circuits) of the column drivers. In general, the voltage relationship is as follows:

$$V0 \leq V1 \leq V2 \leq V3 \leq V4$$

Each D/A converter circuit has a data latch that releases V0-V4 to the summing amplifier according to the instructions from the Controller logic block. The output of the D/A converter circuit sets the voltage applied to a specific cell to control the 'brightness' level of the individual pixel. Note that the levels of brightness and color available are dependent on the complexity of the column drivers.

Although a TFT LCD panel's input waveforms may indicate a digital device, the glass panel is not. The liquid crystal lattice reacts to AC voltage waveforms; therefore, the column driver's D/A converter circuit converts the V0-V4 DC voltages into the respective AC voltage output. The AC voltage controls the amount of light released through the panel. Through the R-G-B subpixels, the color and brightness of each pixel is controlled by this mechanism. The relationship between the emitted light intensity versus the applied voltage is non-linear, and this response curve is called the Gamma Curve. Figure 7b shows how the Gamma Curve correlates the differential voltage with the light transmission levels for a pixel cell (transparency increases from right to left).

Each panel type has a different gamma response curve. For this reason, all TFTs with control electronics are calibrated to the panel's specific Gamma Curve.

Note that to generate the differential voltage, an equal and opposite AC voltage waveform must be generated, as shown in Figure 7b. The alternate polarity characteristic is critical since the net voltage at each pixel must be 0 V to avoid damage to the liquid crystal. The damage is typically displayed as burned-in images or color areas in the active area of the TFT LCD panel.

The greyscale generator circuit outputs the reference DC voltages for V0-V4 so the column drivers can generate color and contrast gradients. This gradient is essentially the Gamma Curve; some powerful TFT controller-driver IC's have built-in functional capabilities allowing the designers to soft-code their Gamma Curve by calibrating the gamma function in the software.

3.2   PANEL STABILITY (REV and VCOM)

In Figure 7b, REV and VCOM can be seen to influence the Gamma Curve. However, REV and VCOM play another, more critical, role in a TFT panel operation – to ensure the TFT panel maintain net zero DC voltage throughout its operation. Please note REV is used to generate VCOM.

Figure 8 shows the top-level REV/VCOM block diagrams and the circuitry in a TFT panel.
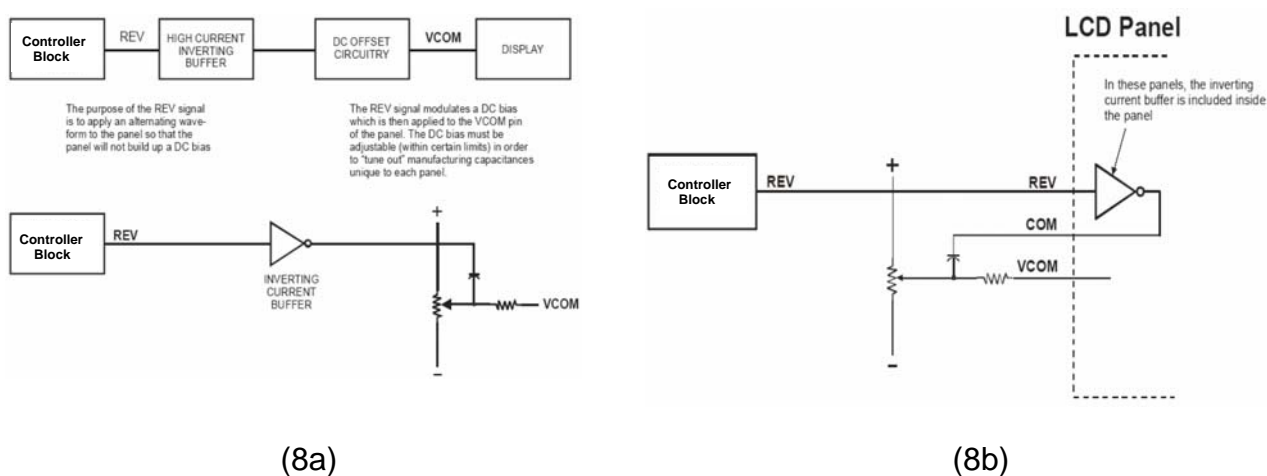
(8a)

(8b)

Figure 8: REV and the corresponding generated VCOM signal

Figure 8a shows the high-level block diagram of the role of REV and VCOM signals. The DC offset and the buffer inverter blocks are calibrated to reflect the capacitance of the LCD panel, among other panel specifications. Figure 8b shows the actual circuit in an LCD panel. The REV/COM/VCOM circuit are contained inside the row/column drivers. The REV waveform is inverted and modulated to generate the VCOM waveform.
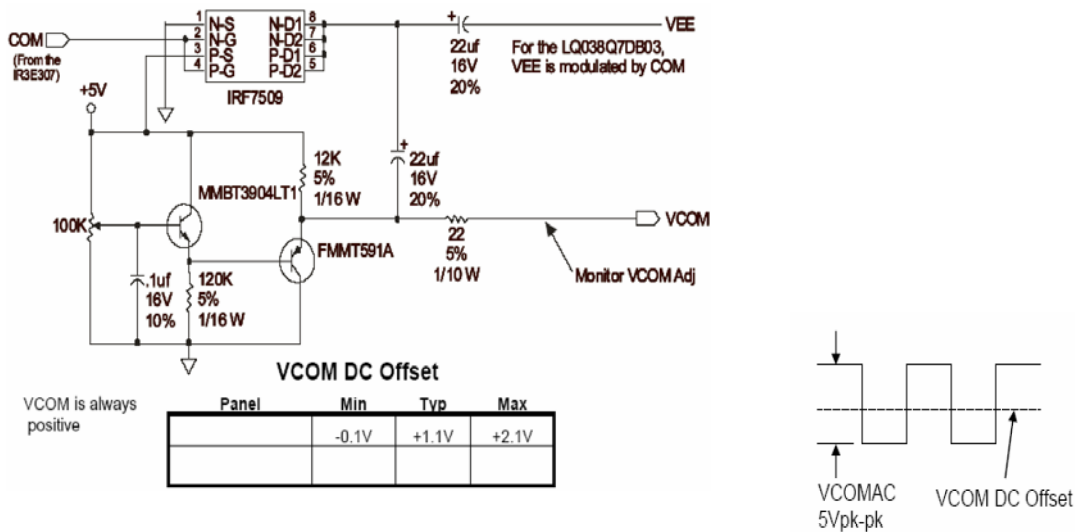
Figure 9: VCOM circuit: DC offset, VCOM adjustment, and
VEE modulation

Figure 9 shows a typical VCOM circuit. VCOM needs to be adjusted to match the capacitance and performance specifications of the TFT panel to maximize contrast and minimize flickering. Therefore, the VCOM circuit is tweaked during panel production to ensure consistent performance. Note that in Figure 9's example, the circuit is constructed to output a typical +1.1V DC Offset. In reality, panels sometimes require a net DC offset to achieve optimum performance due to impurities and other production issues. In addition, VCOM is used to modulate VEE to prevent random DC build-ups.

VCOM is available is some TFT panels as either a programmable function or a pinout in the interface. It is used to adjust the panels to maximize contrast and minimize flickering during operation. VCOM is used to optimize panel performance by conducting a greyscale checkup.
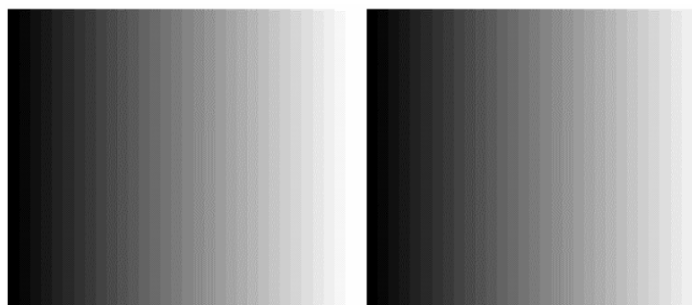
Using the greyscale gradient image, adjust VCOM until pure black is at its optimum intensity. Then adjust VCOM to minimize noise and flickering in the white section as much as possible. A compromise needs to be attained by the TFT panel user.

4 TFT VOLTAGE DRIVE CIRCUITRY

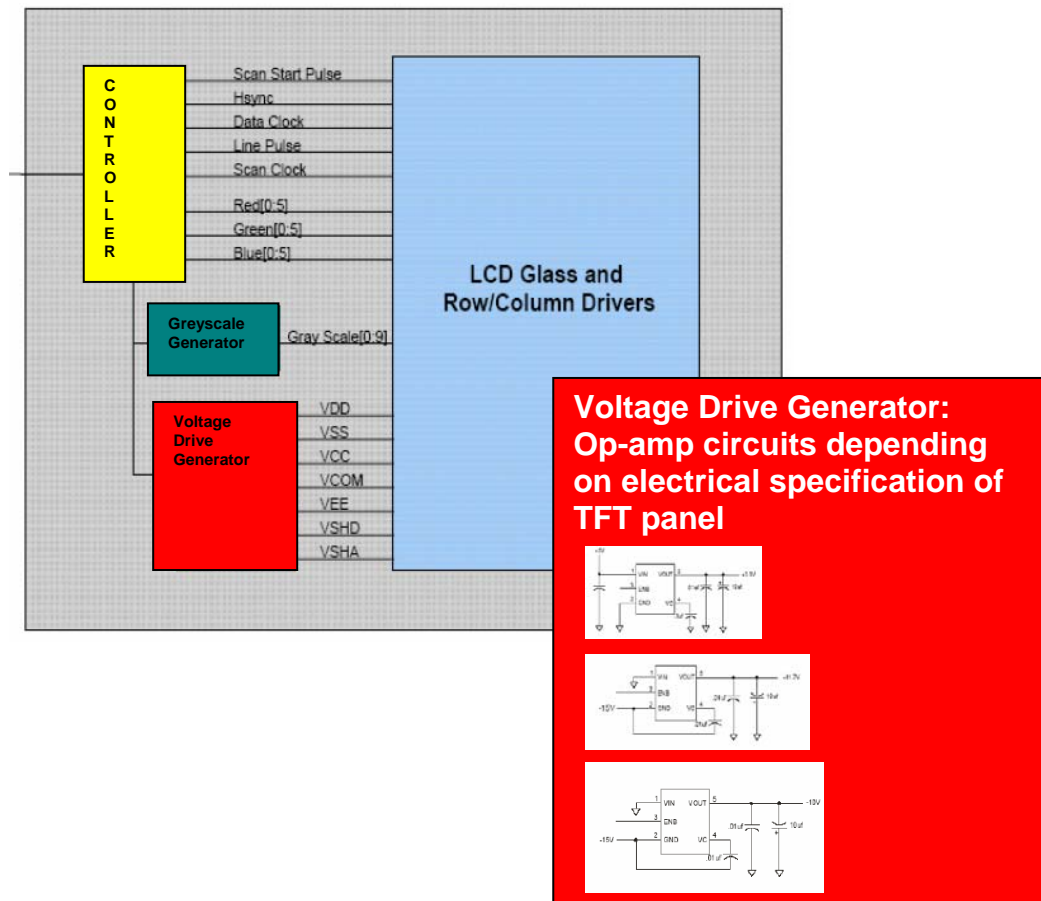## 4.1   VOLTAGE DRIVE GENERATOR

Figure 8: Voltage Drive Generator: generates required supply
voltages for row/column drivers and the greyscale generator block

The Voltage Drive Generator block creates the required supply voltages for
the row/column drivers and the greyscale generator depending on the specification of
the TFT LCD panel. This block is customized to generate the supply voltage
waveforms according to the timing/signal specifications of the row/column drivers and
the electrical specifications of the TFT LCD panel.

Typical supply voltages generated include:

- VDD: positive voltage supply for TFT LCD drive
- VSS: negative voltage supply for TFT LCD drive
- VCC: Gate drive logic voltage (row drivers) [equal to -VEE]
- VEE: Gate drive logic to create the differential for net zero voltage.

- VSHD: Source logic supply voltage (column drivers)
- VSHA: Analog voltage source for the D/A converter circuit

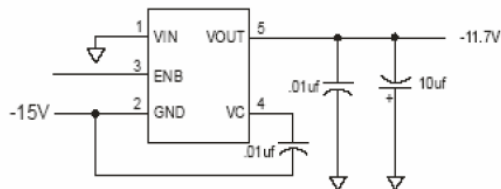## 4.2   SAMPLE VOLTAGE DRIVE CIRCUITS

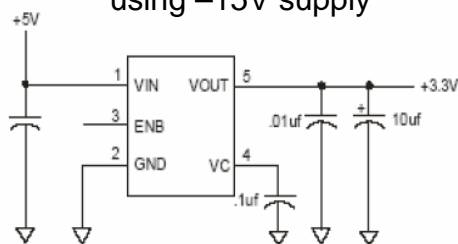Figure 9b: -11.7V supply op-amp circuit
using –15V supply

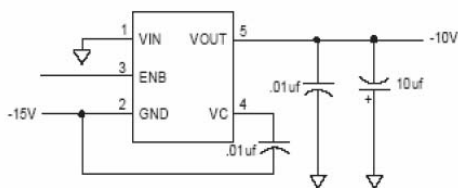Figure 9a: 3.3V supply op-amp circuit

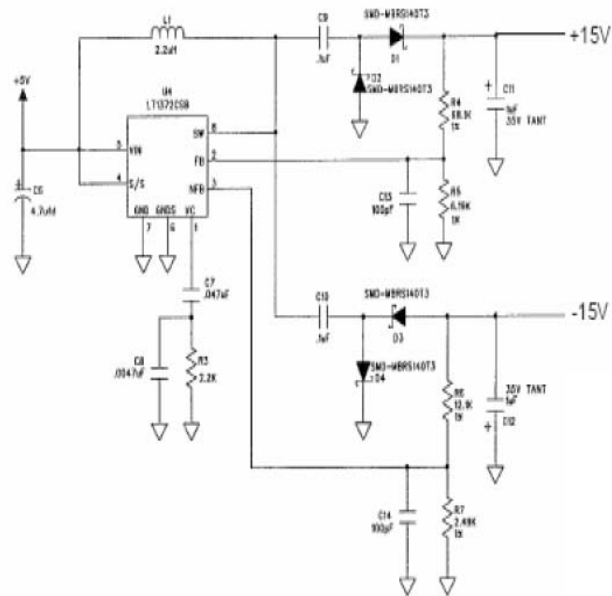Figure 9c: -10V supply op-amp circuit
using –15V supply

Figure 9d: +15V and –15V supply op-amp
circuitry using +5V supply

Depending on the TFT glass panel's supply voltage and the row/column driver's specifications, various supply circuits are used to generate the appropriate voltages from the global input voltage. Some op-amp voltage circuit examples are shown in Figures 9a-d.

Today's mixed-signal fabrication processes allow IC vendors to develop powerful system-on-chip (SOC) TFT controllers that house both the digital controller logic blocks and the analog greyscale generator/power supply generator blocks. These SOC controllers are generally available for small size and portable TFTs. For larger sizes, the TFT array requires multiple column and row drivers, making the processing and power supply logic too large for an SOC to handle. Therefore, in large size TFTs such as notebook TFT LCDs, the blocks tend to be separated into individual IC's: (1) the TFT processor controller, (2) the greyscale generator IC, and (3) the power supply generator IC.

5 POWER SEQUENCING

5.1 POWER SEQUENCING

TFT LCD panels are sensitive to power sequences during power up and power down periods, so it is critical to follow the recommended power-up and power-down sequences to extend and protect the panel's operational lifetime.

Figure 10 is a typical TFT's power supply sequence during a typical panel ON-OFF operation cycle.
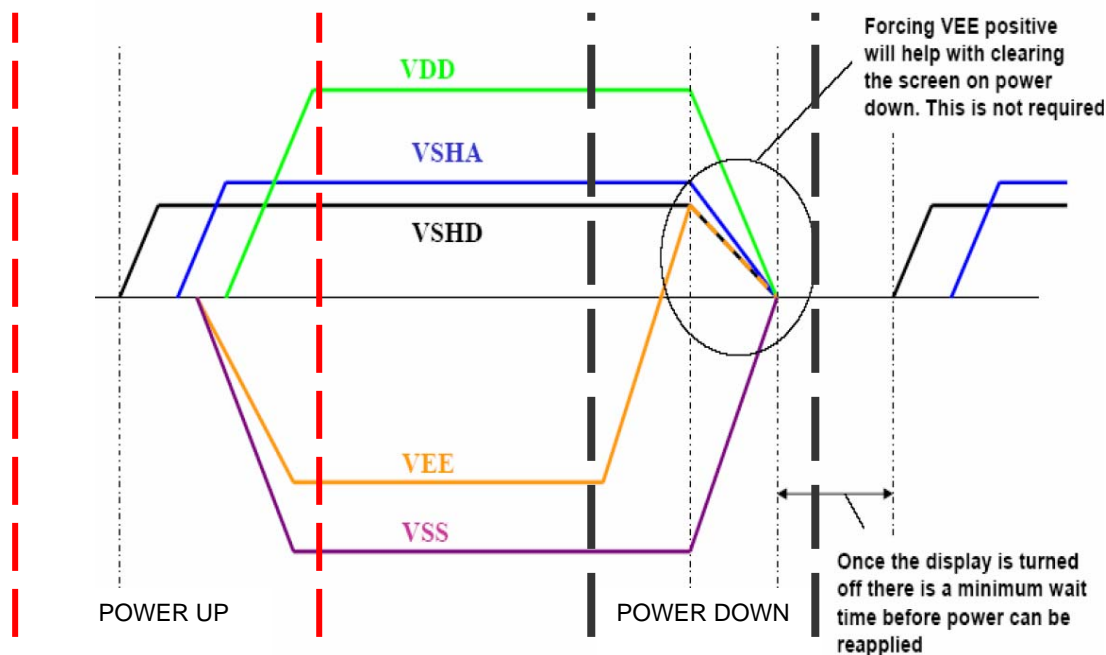

Figure 10: TFT Power Supply Sequence waveform of a typical panel ON-OFF operation cycle

Power Up Period:

During power up, it is critical that VDD, VEE and VSS are activated either simultaneously with or after VSHD is powered up. This sequence activates the row/column drivers before the controller starts sending instructions, to prevent unexpected shocks to the row/column drivers during their power-up. This helps protect the TFT glass panel from any net-voltage damage as well.

Power Down Period:

If you are using a transmissive TFT display, the power down sequence is negligible, since when you turn the backlight off, you will only see a dark screen. If you are using a transflective or reflective TFT panel, then the image will still be visible when the backlight is off. This situation may create an undesirable product.

To solve this problem and create a clean power-down process, it is recommended to follow the clean power sequence below:

1. Display a complete white screen to the panel.
2. Then follow the power sequence as shown in Figure 10.
   a. Ramp Vee up until it reaches VSHD. This process helps clear the screen during power down to prevent any residual images.
   b. Simultaneously bring all power supplies (VDD, VSS, VEE, VSHD, VSHA) all down to net zero voltage to achieve complete shutdown.

6 SUMMARY

This paper summarizes the basic building blocks of the drive electronics behind the TFT LCD panel. The controller, the greyscale generator and voltage drive generator were discussed in detail. In addition, several tips and details for the driving interface of controller-driven TFTs were given in each of the sections. Finally, a primer on safe power-on and clean power-off sequences is reviewed so engineers can design in TFT LCDs with efficient and optimized applications.